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10/776,101	02/11/2004	Kim C. Hardee	UMI-360	2835

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EXAMINER	
YOHA, CONNIE C	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/776,101	HARDEE, KIM C.	
	Examiner	Art Unit	
	Connie C. Yoha	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/11/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Connie C. Yoha

CONNIE C. YOHA
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office acknowledges receipt of the following items from the Applicant:

Papers submitted under 35 U.S.C. 119(a)-(d) have been placed of record in the file.

Information Disclosure Statement (IDS) filed on 4/15/04 was considered.

2. Claims 1-16 are presented for examination.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, in claim 1, 4, 5, 7, 14 and 16 the limitation of "driving a gate terminal of least one element of said output stage to a level above that of said supply voltage source" must be shown or the feature(s) canceled from the claim(s). Such features cannot be seen from the figures. It is not understood by the examiner how gate terminal of the output circuit 224 able to receive a voltage level of **above** or **higher** than the supply voltage source.

No new matter should be entered.

Specification

4. The specification lacks the description of the limitation of claim 1, 4, 5, 7, 14 and 16 of "driving a gate terminal of least one element of said output stage to a level above/higher than that of said supply voltage source". It is therefore very confusion to interpret such claims limitation. For example, starting line 4, page 10 of the specification, it explains the detailed operation circuitry of how the gate of the N-channel

output transistor in the output stage 224 is driven below Vss (e.g. –0.3) in sleep mode, but it only mentioned that the principles of the present invention would likewise pertain to those circuit implementation wherein the gate of the output P-channel transistor of the output stage 224 were also, or alternatively, driven above Vcc (e.g. Vcc + 0.3V). It does not describe how it achieves this concept. Examiner believe that driving a voltage below Vss and driving a voltage above Vcc to the gate terminal of the output stage transistors has very different concepts and required different circuitry implementation. Therefore, the description of the functionality of the circuit implementation wherein the gate of the output P-channel transistor of the output stage 224 operates, or alternatively, driven above Vcc (e.g. Vcc + 0.3V) is needed to be clarified.

Claim Rejections - 35 USC ∋ 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim are rejected under 35 U.S.C. 102(b) as being anticipated by Arimoto, Pat. No. 6100563.

With regard to claim 1, Arimoto discloses a power-gating technique for an integrated circuit device having a sleep mode of operation comprising: providing an output stage (fig. 2, stage element 3) coupled between a supply voltage source (fig. 2,

Vcc at N1) and a reference voltage source (fig. 2, Vss at N2) (col. 6, line 23-28); and driving a gate terminal of least one element (fig. 2, transistor 4 of stage element 3) of said output stage to a level above that of said supply voltage source (fig. 2, Vpp passed through the switch 6b and 6c to node N1) or below that of said reference voltage source (fig. 2, Vbb passed through the switch 7b and 7c to node N2) (col. 6, line 34-53 and col. 7, line 8-19) in said sleep mode of operation (col. 7, line 20-23).

With regard to claim 2, Arimoto discloses wherein said output stage comprises series coupled P-channel (fig. 2, transistor 4 of inverter 3) and N-channel transistors (fig. 2, transistor 5 of inverter 3) coupled between said supply voltage source (fig. 2, Vcc at node N1) and said reference voltage source (fig. 2, Vss at node N2).

With regard to claim 3, Arimoto discloses wherein said gate terminal of said N-channel transistor (fig. 2, transistor 5 of inverter 3) is driven below said reference voltage level (fig. 2, Vbb passed through the switch 7b and 7c to node N2) (col. 6, line 34-43 and 7, line 8-19) while in said sleep mode (col. 7, line 20-23).

With regard to claim 4, Arimoto discloses wherein said gate terminal of said P-channel transistor (fig. 2, transistor 4 of inverter 3) is driven above said supply voltage level (fig. 2, Vpp passed through the switch 6b and 6c to node N1) (col. 6, line 43-53 and col. 7, line 8-19) while in said sleep mode (col. 7, line 20-23).

With regard to claim 5, Arimoto discloses a circuit comprising: an output stage (fig. 2, inverter 3) comprising first and second series coupled transistors (fig. 2, transistor 4 and 5) coupled between a supply voltage source (fig. 2, Vcc at N1) and a reference voltage source (fig. 2, Vss at N2) (col. 6, line 23-28), said output stage

comprising an input terminal (fig. 2, output of inverter 2) and an output terminal thereof (fig. 2, Vout); a power-gating circuit (fig. 2, the switch between 6b and 6c) coupled to a stage preceding said output stage (fig. 2, node N1 to inverter 2) for applying a voltage level (fig. 2, Vpp passed through the switch 6b and 6c at Node N1 through the inverter 2 to the gate of inverter 3) (col. 6, line 43-53 and col. 7, line 8-19) (col. 7, line 20-23).

With regard to claim 6 and 12, Arimoto discloses wherein said output stage comprises a cmos inverter (fig. 2, inverter 3) and said first transistor comprises a P-channel transistor (fig. 2, transistor 4 of inverter 3).

With regard to claim 8, Arimoto discloses a circuit comprising: an output stage (fig. 2, stage 3) comprising first and second series coupled transistors (fig. 2, transistor 4 and 5) coupled between a supply voltage source (fig. 2, Vcc at N1) and a reference voltage source (fig. 2, Vss at N2) (col. 6, line 23-28), said output stage comprising an input terminal (fig. 2, output of inverter 2) and an output terminal thereof (fig. 2, Vout); a power-gating circuit (fig. 2, the switch between 6b and 6c) coupled to a stage preceding said output stage (fig. 2, inverter 2) for applying a voltage level (fig. 2, Vbb) to a gate terminal of said second transistor less than that of said reference voltage source (fig. 2, Vbb passed through the switch 7b and 7c at Node N2 through the inverter 2 to the gate of inverter 3) in response to a sleep mode of operation (col. 6, line 34-43 and 7, line 8-19) (col. 7, line 20-23).

With regard to claim 9, Arimoto discloses wherein said output stage comprises a cmos inverter (fig. 2, inverter 3) and said second transistor comprises a N-channel transistor (fig. 2, transistor 5 of inverter 3) (also with regard to claim 13).

With regard to claim 11, Arimoto discloses an integrated circuit device including a power-gated write data driver circuit for a memory array, said driver circuit comprising: at least a first stage (fig. 2, inverter 2) coupled between a supply voltage source (fig. 2, Vcc at N1) and a power-gated reference voltage line (fig. 2, Vss at N2) (col. 6, line 23-28); an output stage (fig. 2, inverter 3) coupled between a supply voltage source (fig. 2, Vcc at N1) and a reference voltage source (fig. 2, Vss at N2) (col. 6, line 23-28), an input to said output stage being coupled to an output of said at least said first stage (fig. 2, output of inverter 2 input to the inverter 3); and a power-gating circuit (fig. 2, the switch between 7b and 7c) coupled to a stage preceding said output stage (fig. 2, Node N3 of inverter 2) for driving said input to a level lower than that of said reference voltage source level (fig. 2, Vbb passed through the switch 7b and 7c at Node N2 through the inverter 2 to the gate of inverter 3) (col. 6, line 34-43 and col. 7, line 8-19) in response to a sleep mode of operation (col. 7, line 20-23).

With regard to claim 14, Arimoto discloses an integrated circuit device including a power-gated write data driver circuit for a memory array, said driver circuit comprising: at least a first stage (fig. 2, inverter 2) coupled between a reference voltage source (fig. 2, Vss at N2) and a power-gated supply voltage line (fig. 2, Vcc at N1) (col. 6, line 23-28); an output stage (fig. 2, inverter 3) coupled between a supply voltage source (fig. 2, Vcc at N1) and a reference voltage source (fig. 2, Vss at N2) (col. 6, line 23-28), an input to said output stage being coupled to an output of said at least said first stage (fig. 2, output of inverter 2 input to the inverter 3); and a power-gating circuit (fig. 2, the switch between 6b and 6c) coupled to said input of said output stage (fig. 2, inverter 2)

for driving said input to a level greater than that of said supply voltage source (fig. 2, Vpp passed through the switch 6b and 6c at node N1 through the inverter 2 to the gate of the inverter 3) (col. 6, line 43-53 and 7, line 8-19) in response to a sleep mode of operation (col. 7, line 20-23).

Claim Rejections - 35 USC ∋ 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimoto, Pat. No. 6100563.

With regard to claim 7, Arimoto, as applied in prior rejection, disclosed all claimed subject matter except he is silence about wherein said voltage level applied to said gate terminal of said first transistor comprises substantially said supply voltage source level plus 0.3V. However, since Arimoto does disclose that the voltage level applied to the terminal of the first transistor is a boosted voltage Vpp (fig. 2, Vpp) (col. 6, 16-17), an ordinary skill in the art would recognized that Vpp voltage would preferably be a voltage of a supply voltage plus a threshold voltage of the transistor, which in this case the threshold voltage of a typically transistor is 0.3 V. Therefore, it would have been

obvious for one having an ordinary skill in the art at the time the invention was made to apply a boosted Vpp voltage of Arimoto's to the gate terminal of the transistor that have substantially the supply voltage source level plus 0.3V. to increase the driving capability so that the integrated memory device can operate at high speed under low power consumption (col. 2, line 61-col. 3, line 15).

With regard to claim 10, Arimoto, as applied in prior rejection, disclosed all claimed subject matter except he is silence about wherein said voltage level applied to said gate terminal of said second transistor comprises substantially said reference voltage source level minus 0.3V. However, since Arimoto does disclose that the voltage level applied to the terminal of the second is a negative voltage Vbb (fig. 2, Vbb) (col. 6, 17-20), an ordinary skill in the art would recognized that Vbb voltage would preferably be a voltage of a reference voltage minus a threshold voltage of the transistor, which in this case the threshold voltage of a typically transistor is 0.3 V. Therefore, it would have been obvious for one having an ordinary skill in the art at the time the invention was made to apply a negative Vbb voltage of Arimoto's to the gate terminal of the transistor that have substantially the reference voltage source level minus 0.3V to increase the driving capability so that the integrated memory device can operate at high speed under low power consumption (col. 2, line 61-col. 3, line 15).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Yang et al (6670939), Tsukagoshi et al (6072333), Shamlou et

al (6307408) and Takashima (5541885) disclose a memory device having standby mode.

8. When responding to the office action, Applicants' are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1799. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, Amir Zarabian, can be reached at (571) 272-1852. The fax phone number for this Group is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov should you have questions on access to the Private Pair system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Yoha

February 2006

CONNIE C. YOHA
PRIMARY EXAMINER